CLAIMS:

1. An apparatus for reducing the rate of temperature change in a processing device due to a change in operational state for the processing device, the apparatus including:

(a) a power transitioning arrangement for transitioning power dissipation in the processing device between a low power dissipation level and a high power dissipation level in response to a change in a power state signal, the high power dissipation level being relatively greater than the low power dissipation level;

(b) a cooling system alternatively providing a low thermal impedance for the processing device and a relatively higher, high thermal impedance for the processing device; and

(c) a cooling system controller for placing the cooling system at the high thermal impedance in conjunction with a transitioning from the high power dissipation level to the low power dissipation level, and for placing the cooling system at the low thermal impedance in conjunction with a transitioning from the low power dissipation level to the high power dissipation level.

2. The apparatus of Claim 1 wherein the power transitioning arrangement includes a delay element for delaying the transitioning between power dissipation levels relative to a change between the low thermal impedance and the high thermal impedance.

3. The apparatus of Claim 1 wherein the power transitioning arrangement includes:

(a) a frequency divider connected to receive a system clock for the processing device and providing a frequency divider output; and

(b) a frequency controller operatively connected to the frequency divider for controlling the frequency division function applied to the system clock by the frequency divider.

4. The apparatus of Claim 3 wherein the power transitioning arrangement further includes a frequency divider bypass and a system clock output.

5. The apparatus of Claim 3 further including:

(a) an additional frequency divider connected to receive the system clock signal and providing an additional frequency divider output, the additional frequency divider being operatively connected to the frequency controller; and

(b) a multiple clock distribution system associated with the processing device for distributing both the frequency divider output and the additional frequency divider output to the processing device.

6. The apparatus of Claim 1 wherein the power state signal comprises a wake/sleep signal and the high power dissipation level corresponds to a maximum clock rate for the processing device while the low power dissipation level corresponds to a sleep clock rate for the processing device.

7. The apparatus of Claim 1 wherein the cooling system comprises a heat sink and a fan positioned to affect airflow over the heat sink.

8. The apparatus of Claim 7 wherein the cooling system further includes a cooling system switching device connected to receive the awake/asleep signal for the processing device and a power on/off signal for a processing system including the processing device.

9. The apparatus of Claim 1 further including a power transitioning bypass arrangement for causing the processing device to operate at the high power dissipation level substantially immediately upon receipt of a power transitioning bypass signal.

10. A processing system having at least one processing element adapted to operate using a clock input, and also having a system power management arrangement providing alternatively a high power state signal and a low power state signal, the processing system including:

(a) a system clock arrangement providing the clock input to the processing system, the system clock arrangement for transitioning from a high clock rate at the clock input to a relatively slower, low clock rate at the clock input in response to a change from the high power state signal to the low power state signal, the system clock arrangement also for transitioning from the low clock rate at the clock input to the high clock rate in response to a change from the low power state signal to the high power state signal;

(b) a cooling system providing alternate thermal impedance states for transferring heat from the processing system, the thermal impedance states including a high thermal impedance state and a relatively lower, low thermal impedance state; and

(c) a cooling system controller operably connected to the cooling system for changing the thermal impedance state of the cooling system from the high thermal impedance state to the low thermal impedance state in response to a change from the low power state signal to the high power state signal, and for changing the thermal impedance state of the cooling system from the low thermal impedance state to the high thermal impedance state in response to a change from the high power state signal to the low power state signal.

11. The apparatus of Claim 10 wherein the power transitioning arrangement includes a delay element for delaying the transitioning between power dissipation levels relative to a change between the low thermal impedance and the high thermal impedance.

12. The apparatus of Claim 10 wherein the power transitioning arrangement includes:

(a) a frequency divider connected to receive a system clock for the processing device and providing a frequency divider output; and

(b) a frequency controller operatively connected to the frequency divider for controlling the frequency division function applied to the system clock by the frequency divider.

13. The apparatus of Claim 12 wherein:

(a) the processing system includes a second processing element and the system clock arrangement further includes an additional frequency divider connected to receive the system clock and providing an additional divider output; and

(b) the processing system further includes a multiple clock distribution system for distributing both the frequency divider output and the additional frequency divider output to the processing system.

14. The apparatus of Claim 10 wherein the cooling system comprises a heat sink and a fan positioned to affect airflow over the heat sink.

15. The apparatus of Claim 14 wherein the cooling system further includes a cooling system switching device connected to receive the wake/asleep signal for the processing device and a power on/off signal for a processing system including the processing device.

16. The apparatus of Claim 10 further including a power transitioning bypass arrangement for causing the processing device to operate at the high power dissipation level substantially immediately upon receipt of a power transitioning bypass signal.

17. A method for reducing the rate of temperature change in a processing device as the processing device undergoes a change in operational state, the method including the steps of:

(a) transitioning power dissipation in the processing device between a low power dissipation level and a high power dissipation level in response to a change in a power state signal, the high power dissipation level being relatively greater than the low power dissipation level; and

(b) placing a cooling system for the processing device at a high thermal impedance in conjunction with a transitioning from the high power

dissipation level to the low power dissipation level, and placing the cooling system at the low thermal impedance in conjunction with a transitioning from the low power dissipation level to the high power dissipation level.

18. The method of Claim 17 further including the step of delaying the transitioning between power dissipation levels relative to a change between the low thermal impedance and the high thermal impedance.

19. The method of Claim 17 wherein the step of transitioning power dissipation includes gradually modifying the clock rate of the processing device.

20. The method of Claim 20 wherein the step of transitioning power dissipation includes modifying the power dissipation of different processing elements in the processing device at different times.